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APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Dong Yeal Keum**, a citizen of Republic of Korea, residing at #206-1004 Daewoo 2-cha Apt., Jeungpo-dong, Icheon-si Gyeonggi-do 467-719 KOREA have invented a new and useful **METHOD FOR FABRICATING A TRANSISTOR**, of which the following is a specification.

METHOD FOR FABRICATING A TRANSISTOR

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates generally to semiconductor devices and, more particularly, to a method for fabricating a transistor with an LDD (lightly doped drain) region.

BACKGROUND

[0002] In general, with the rapid spread of intelligent devices such as computers, semiconductor devices are rapidly being developed. Recently, semiconductor devices are required to have high storage-capability as well as to operate at a high speed. To meet these requirements, technologies for manufacturing semiconductor devices are being developed to satisfy the higher demand for integration, reliability, operating speed. As a result of this trend, semiconductor devices with a micro pattern are being developed and the channel length of transistors on a semiconductor substrate is being rapidly reduced.

[0003] Fig. 1 illustrates a cross-sectional view of a transistor made according to a conventional fabricating method. As shown in Fig. 1, a transistor according to the conventional method comprises a gate electrode 12, a source/drain region 16a and 16b with an LDD (lightly doped drain) region. Spacers 14 are formed on the sidewalls of the gate electrode 12, on a substrate 10. The gate electrode 12 comprises a gate oxide 12b and a gate poly 12a. In addition, a pocket junction region 18 is formed at the sides of the lightly doped drain (LDD) region of the source/drain region 16a and 16b. The pocket junction region 18 can mitigate the occurrence of punch-through and current leakage in a transistor.

[0004] However, the punch-through in the bulk of a silicon wafer is more likely to occur as transistor size is scaled down. Such punch-through cannot be prevented only

by the pocket junction. Moreover, the functional limitations of ion implantation equipment present difficulty in reducing the junction depth without limit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figs. Fig. 1 illustrates a cross-sectional view of a transistor made according to a conventional fabricating method.

[0006] Figs. 2a through 2d illustrate, in cross-sectional views, an example fabricating process of an example transistor.

DETAILED DESCRIPTION

[0007] As described in greater detail below, an example fabricating method is capable of reducing the junction depth of a source/drain region with an LDD region, as a transistor's size decreases. More specifically, one example method forms a gate electrode on a substrate with an active region defined by a device isolation layer, forms a first preliminary source/drain region and a pocket junction region through a first ion implantation process using the gate electrode as a mask, the pocket junction region being formed under the first preliminary source/drain region. In addition, the example method forms a first oxide layer with uniform thickness on the substrate including the gate electrode, forms a nitride layer with uniform thickness on the first oxide layer, forms a second oxide layer over the nitride layer, forms spacers on sidewalls of the gate electrode by performing an etch back process for the second oxide layer, forms a second preliminary source/drain region through a second ion implantation process using the spacers as a mask, removes the nitride layer and the first oxide layer on the surface of the substrate, and diffuses the implanted ions only in a horizontal direction of the substrate by performing a thermal treatment process for the resulting substrate. In addition, the example fabricating method may further

comprise performing a thermal treatment process prior to the removal of the nitride layer and the first oxide layer.

[0008] By forming spacers consisting of a first oxide layer, a nitride layer, and a second oxide layer on the sidewalls of a gate electrode and performing a thermal treatment process, the example fabrication methods described herein may easily reduce the junction depth of a source/drain region with an LDD region.

[0009] Referring to Fig. 2a, a substrate 20 with an active region defined by a device isolation layer 22 is provided. The device isolation layer 22 is preferably a trench oxide layer. The trench oxide layer is generally used for device isolation in fabricating a semiconductor device with a micro pattern. Another example of the device isolation layer is a field oxide layer.

[0010] Then, an oxide layer and a polysilicon layer are formed in sequence on the substrate 20. A photoresist pattern is formed on the polysilicon layer by photolithography. The oxide layer and the polysilicon layer are etched using the photoresist pattern as a mask to form a gate poly 24b and a gate oxide 24a. As a result, a gate electrode 24 comprising the gate poly 24b and the gate oxide 24a is formed on the substrate 20.

[0011] Next, a first ion implantation process is performed using the gate electrode 24 as a mask to form a first preliminary source/drain region 26 at both sides of the gate electrode 24 in the substrate 20. Here, to prevent surface punch-trough in a transistor, a pocket junction region 27 is formed under the first preliminary source/drain region 26.

[0012] Referring to Fig. 2b, a first oxide layer 28 with uniform thickness is formed on the substrate 20 including the gate electrode 24. A nitride layer 29 with uniform thickness is formed on the first oxide layer 28. A second oxide layer is formed over

the nitride layer 29. Then, an etch back process is applied to the second oxide layer to form spacers 30 on the sidewalls of the gate electrode 24. Here, the nitride layer 29 functions as an etch-stop layer during the etch back process.

[0013] Referring to Fig. 2c, a second ion implantation process is performed using the spacers 30 as a mask to form a second preliminary source/drain region in the substrate 20. During the ion implantation process, the depth of the ion implantation is controlled by means of the nitride layer 29 and the first oxide layer 28. Therefore, the implanted ions are placed in a shallower area of the substrate 20. Then, a thermal treatment process may be performed for the resulting substrate 20, additionally. Through the thermal treatment, the ions implanted in the substrate 20 are diffused along with the surface of the substrate 20 because the nitride layer 29 prevents the diffusion of ions.

[0014] Referring to Fig. 2d, the nitride layer 29 and the first oxide layer 28 on the surface of the substrate are removed. As a result, the gate electrode 24 with a spacer structure is formed on the structure 20. The spacer structure is a multi-layer structure comprising a first oxide layer 28a, a nitride layer 29a, and a second oxide layer 30.

[0015] Next, a thermal treatment process is performed for the resulting substrate 20. Through the thermal treatment, the junction depth of a source/drain region 26a is easily controlled. In other words, the source/drain region 26a with a shallow junction is formed. The shallow junction is formed because the nitride layer 29a of the spacer structure prevents diffusion of the ions during the thermal treatment. A pocket junction region 32 remains at the sides of the LDD (lightly doped drain) region of the source/drain region 26a.

[0016] Therefore, the example fabrication method can easily form a source/drain region with shallow junction. The example fabrication method is applicable to a

fabricating process of a semiconductor device being continuously scaled down (i.e., made using smaller pattern features). In addition, the example fabrication method may be used to overcome the functional limitations of semiconductor fabricating equipments by a fabrication process that embodies a source/drain region with shallow junction. Consequently, the present invention can enhance productivity and reliability in fabricating a semiconductor device.

[0017] Although certain methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. To the contrary, this patent covers all embodiments fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.